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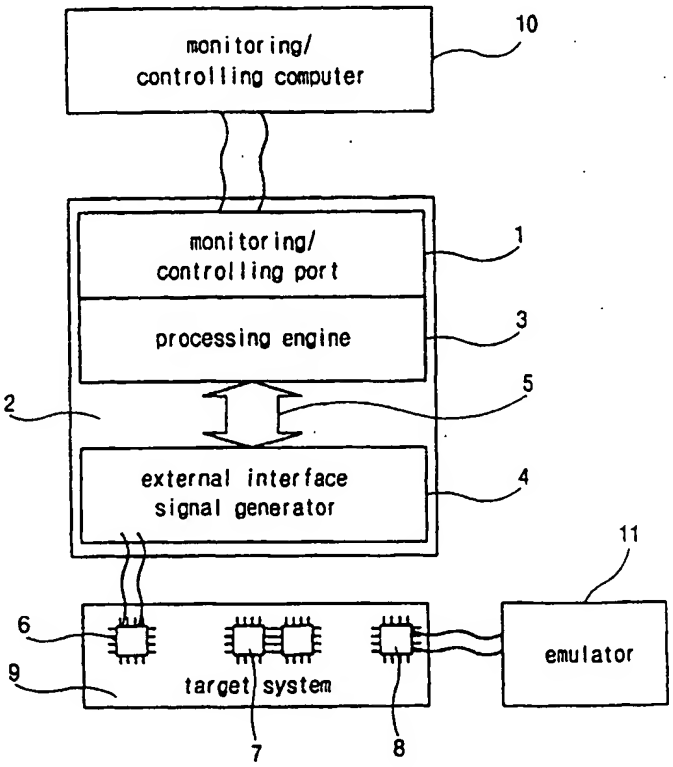
(54) Title: VLSI EMULATOR COMPRISING PROCESSORS AND RECONFIGURABLE CIRCUITS

(57) Abstract

Disclosed is an apparatus for verifying a VLSI design at an early stage as well as a later stage, and particularly a VLSI emulator based on processors and reconfigurable chips. The model of the VLSI chip is divided into a functional part and an external interface part. The functional part is executed by a processing module having at least one processor, and the external interface part is executed by an external interface signal processor to generate real pin signals. The external interface part is implemented using reconfigurable circuits by programming the circuits. The communicating between the functional part and the external interface part is accomplished by transmitting and/or receiving control packets composed of control commands and/or or data. The intenal functional part and the external interface part are verified on a target system at an early stage of the VLSI design, which may reduce time for designing the VLSI and verifying and designing whole system.



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VLSI EMULATOR
COMPRISING PROCESSORS AND RECONFIGURABLE CIRCUITS

TECHNICAL FIELD

The present invention relates to an apparatus for verifying a VLSI design through emulation, and more particularly to a VLSI emulator using processors and reconfigurable chips for verifying the functional correctness of the design of a VLSI together with a system to which the VLSI will be attached before manufacturing the design into a chip.

BACKGROUND ART

In general, it is desirable to eliminate all the design errors in a VLSI design procedure before the fabrication of the VLSI chip as the VLSI chip fabrication requires significant time and cost. However, the probability of error in the design of VLSI becomes high according to the complexity of the VLSI and the system to which the VLSI will be attached. Therefore, it is essential to verify the functional correctness of the VLSI within the context of the target system in advance using an emulator.

On the other hand, a conventional emulator is configured to connect Field Programmable Gate Arrays (FPGA) with a reconfigurable network, to emulate a gate-level logic circuit. Such an emulator can verify

a design only at a later stage of the design procedure. The fact that the conventional emulator cannot perform verification at the early stage of the design procedure. Becomes critical especially when the design turnaround time needs to be reduced.

US Patent 4,901,259 issued to Watkins shows an ASIC emulator in which a host computer executes a software model of the whole VLSI, Watkins' ASIC emulator system calculates pin signal values contained in the modeling, and then converts the pin signal values into electrical signals in order to send the values to a socket. Communication between the host computer and the ASIC emulator consists of a lot of pin signal values required for all pins. However, when fast emulation in required such a system becomes problematic due to the following reasons which causes difficulties in various VLSI designs; 1) the host computer uses software which is slow to execute the whole process related to generation of the pin signal used for external interface part; 2) communication speed through an I/O port of a full-fledged host computer is generally very slow as compared with a processor; and 3) the host computer is connected to the ASIC emulator through a cable whose transmission capability may be slow enough to affect the system. In addition, because of employing the host computer, the system should have modules and functions unrelated to emulation, which makes the system unnecessarily bigger.

In this regard the present invention proposes a scheme for enhancing the emulation speed in order to effectively verify the functional

correctness of the design of a VLSI at the early stage of the design procedure. The emulation module of a VLSI being designed is divided into a functional part and an external interface part, where the functional part is executed by a processing module having at least one processor while the external interface part is executed by an external interface signal processor using field-reconfigurable circuits such as FPGA's(Field Programmable Gate Advance) to generate the required pin signals.

DISCLOSURE OF INVENTION

The present invention intends to remove or at least alleviate the above problems with Watkins' ASIC emulator by proposing a VLSI emulator being comprised of processor(s) and reconfigurable circuits(s) which can be used to freely verify a VLSI design at its early stage as well as at the later stage.

Another object of the present invention is to enhance the emulation speed and generate pin signals more timely and appropriately by adopting a processor-based processing module for the functional part of a VLSI while adopting reconfigurable circuits(s) for the external interface part. An interface control packet is employed for communication between the processing module and the reconfigurable circuits(s).

In order to achieve the above-mentioned objectives, the present invention provides an apparatus for verifying the functional part and the

external interface part of a VLSI, separately, using a VLSI emulator comprising: a processing module including at least one processor for verifying the functional part of the VLSI; and an external interface signal processor for verifying the external interface part of the VLSI. The external interface signal processor is implemented using reconfigurable circuits to generate the required pin signals. Communication between the processing module and the external interface signal processor consists of commands and data.

In the apparatus, the processing module as comprises at least one processor; and at least one memory such as ROM and/or RAM; and a bus for connecting the processor and the memory.

In the apparatus, the external interface signal processor may comprise a pin signal processing unit having at least one reconfigurable element for performing an external interface model of the VLSI design; a buffer and controller for buffering and synchronizing to fill up the speed gap between the processing module and the pin signal processing unit; a channel for communication of an interface control packet between the processing module and the external interface signal processor; and a socket for connecting the external interface signal processor to a target system to which the VLSI for verification is attached.

The apparatus may further comprise a monitoring/controlling port connected to a monitoring/controlling computer for monitoring and controlling the emulation states externally, downloading a software model

and a monitoring code to the processing module, and reconfiguring the reconfigurable element(s) in the external interface signal processor

BRIEF DESCRIPTION OF DRAWINGS

The objectives and the associated advantages of the present invention can be made more clear from the following description of an implementation example with reference to the associated drawings, in which;

FIG. 1 shows an example for the explanation of the VLSI emulator according to the present invention;

FIG. 2 shows an example of a processor-based processing module; and

FIG. 3 shows an example of an external interface signal processor.

BEST MODE FOR CARRYING OUT THE INVENTION

Hereinafter, a VLSI circuit emulation apparatus and method according to the implementation of the present invention is explained with reference to the accompanying drawings.

FIG. 1 is for illustrating an emulation system (or emulator) and its peripherals according to the present invention.

The model of a VLSI to be verified is divided into a software model which represents the functional part of a VLSI and an external interface model which represents the actions of the VLSI related with the external interface.

As shown in Fig. 1, an emulator denoted as 2 includes a processing module 3 having at least one processor for executing the software model of the functional part, and an external interface signal processor 4 having reconfigurable circuit (e.g. FPGA) to interface with the external hardware according to the external interface model. The processing module 3 transmits a corresponding interface control packet to the external interface signal processor 4 through a channel 5 when there is a need to interface with the external hardware. The external interface signal processor 4 interprets the interface control packet received to generate and transmit a sequence of electrical signals to a target system 9. The external interface signal processor 4 also reads in electrical signals from the target system 9 to interpret and transmit them to the processing module 3.

The target system 9 has a socket 6 to which electrical pin signals as generated from the external interface signal processor 4 are connected. The socket 6 enables the target system 9 to be electrically connected to the target system 9 consisting of other VLSI chip(s) denoted as 7 and other socket(s) 8 connected to another emulators 11 which can be the VLSI emulator described herewith or any other type of emulator.

On the other hand, the emulator 2 can be connected to a host computer 10 through a monitoring/controlling port 1 in order to externally monitor and control the internal state(s) of emulation. In addition, the monitoring/controlling port 1 is used to download the software model of the VLSI chip to be verified from host computer 10 to the processing module 3 and to reconfigure the reconfigurable circuit(s) in the external interface signal processor 4 before the emulation begins.

FIG. 2 is for illustrating an example for the implementation of the processing module 3.

Referring to the figure, the software model for the functional part of a VLSI to be verified is compiled into a form to be executed in a processor 12 in the processing module 3, and then stored in a memory 13 together with a monitoring code. The processor 12 executes the software model in the memory 13. At this time, the software model is divided into a plurality of blocks in order to be possibly executed by a plurality of processors and memories. In addition, a communication channel is provided for communication among a plurality of processors. The memory 13 is composed of ROM and/or RAM, and may have a code, already processed, or receive the code through the monitoring/controlling port 1. When the software model for the functional part of a VLSI to be verified reads or writes a value from/to the target system 9, the processor 12 transmits an interface control packet of the software model to the external interface signal processor 4 through the channel 5. In case of writing

data to the target system 9, the interface control packet is composed of a write command, an address and data to be written. On the other hand, in case of reading data from the target system 9, the interface control packet is composed of a read command and an address. Then, after confirming that the external interface signal processor 4 reads data in the target system 9, the interface control packet is sent to bring the data. The emulation state is controlled and monitored by commands, transmitted from the host computer 10 through the monitoring/controlling port 1.

FIG. 3 is illustrates an example of the implementation of the external interface signal processor 4, where the interface control packet from the processing module 3 through the channel 5 is stored in a buffer 15 through a controller 14. Commands and data of the packet are generated according to the sequence of signals by a pin signal processing unit 16 implemented as a field-reconfigurable circuit as configured in accordance with an external interface model, before they are transmitted to the socket 6. The reconfigurable circuit in the pin signal processing unit 16, which can be implemented as FPGA's(Field Programmable Gate Array), is either reconfigured by a reconfiguring code stored in the memory 13, which can be ROM or a reconfiguration-dedicated ROM/RAM, or downloaded through the monitoring/controlling port 1 before the emulation starts.

In case of reading, the value read from the socket 6 via the pin signal processing unit 16, is stored in the buffer 15, which is then

informed to the processing module 3. After that, the processing module 3 takes the stored value. The buffer 15 plays the role of buffering between the processing module 3 and the pin signal processing unit 16. In case of writing, the pin signal processing unit 16 compiles data in the buffer 15 into a sequence of electrical signals, and transmits them to the socket 6.

INDUSTRIAL APPLICABILITY

The present invention as constructed above enables one to perform the emulation at the early stage of the VLSI design only with the functional description of the VLSI, i.e., before the gate-level or hardware description of the VLSI is available. Therefore, the present invention effectively reduces the time for the development of a VLSI as well as its target system.

CLAIMS

1. An apparatus for emulating a VLSI design comprising:

a processing module having one or more processors to execute a software model of the functional part of the VLSI; and

a reconfigurable module configured as a hardware model of the external interface part of the VLSI design in a plurality of field programmable gates; and

a channel wherein interface control packets composed of commands and data are transferred between said processing module and said reconfigurable module.

2. The apparatus of claim 1, wherein said processing module comprises:

at least one predefined processor; and

at least one memory including ROM and/or RAM; and

a bus for connecting the processor and the memory.

3. The apparatus of claim 1, wherein said reconfigurable module comprises:

a pin signal processing unit configured in a plurality of field programmable gates to generate a sequence of pin signals by processing output data and in accordance therewith receive input data by processing

a sequence of pin signals; and

a set of buffers to store the output data coming from said processing module and the input data coming from said pin signal processing unit; and

a control unit for managing said set of buffers and synchronizing speed difference between said processing module and said pin signal processing unit.

4. The apparatus of claim 1, further comprising a socket for connecting said reconfigurable module to a target system to which the VLSI is attached.

5. The apparatus of claim 1, further comprising a monitoring/controlling port to be connected to a monitoring/controlling computer for monitoring and controlling the state of emulation externally, downloading a software model and a monitoring code to said processing module.

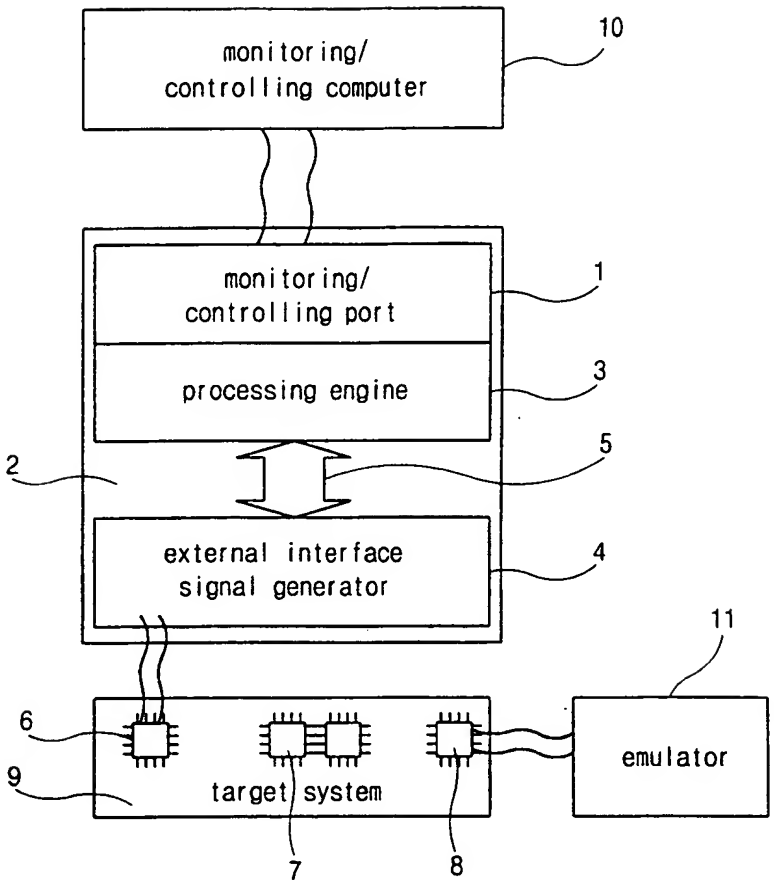
monitoring/
controlling computer
10
monitoring/
controlling port
1
processing engine
3
2
5
external interface
signal generator
4
11
6
9
target system
emulator
7
8

FIG. 1

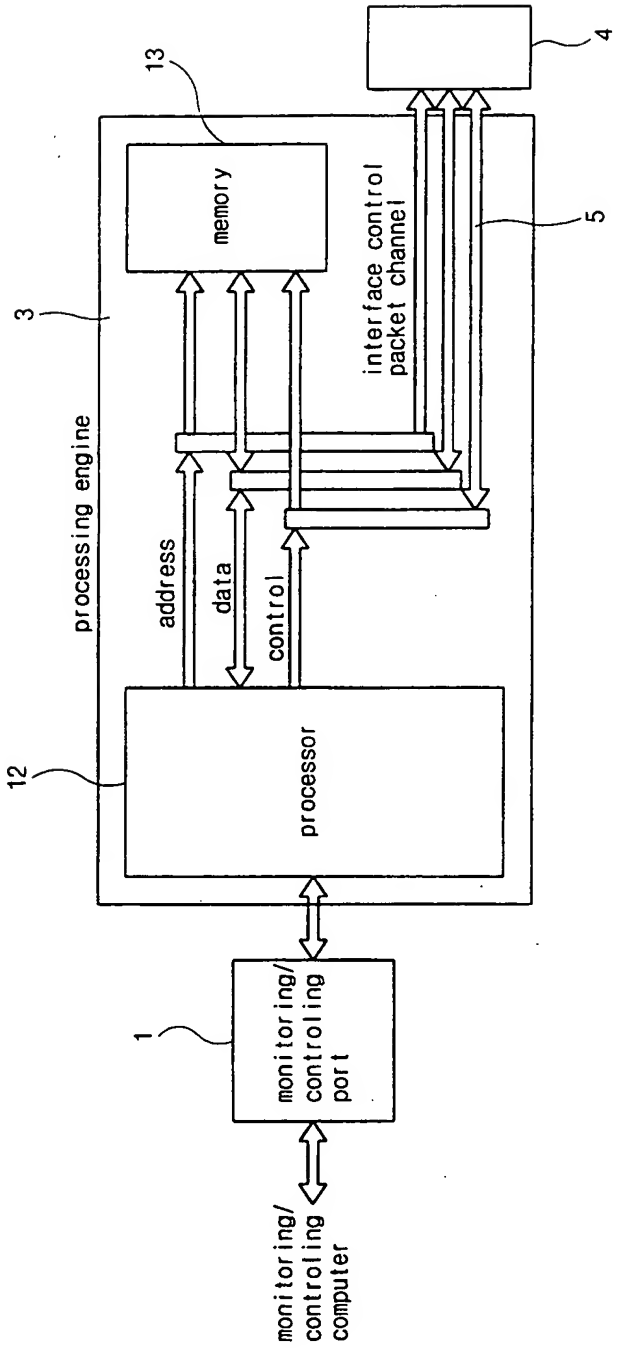
4
13
memory
interface control
packet channel
5
3
processing engine
address
data
control
12
processor
1
monitoring/
controling
port
monitoring/
controling
computer

FIG. 2

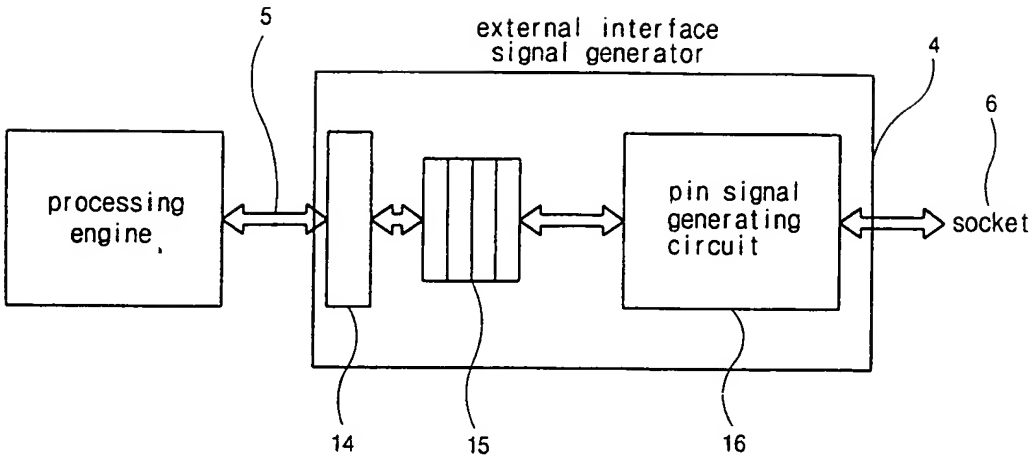
5
external interface
signal generator
4
6
processing
engine
pin signal
generating
circuit
socket
14
15
16

FIG. 3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR 00/00229

CLASSIFICATION OF SUBJECT MATTER

IPC[7]: G 06 F 9/455; 17/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC[7]: G 06 F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5477475 A (SAMPLE et al.) 19 December 1995 (19.12.95) claim1; fig.1.	1-3
A	US 5355528 A (ROSKA et al.) 11 October 1994 (11.10.94) abstract; fig.1,2,3.	1-3
A	US 5329470 A (SAMPLE et al.) 12 July 1994 (12.07.94) claims 1-3; fig.1-5.	1-3
A	US 5546562 A (PATEL) 13 August 1996 (13.08.96) abstract; fig.1.	1-3
A	US 5638531 A (CRUMP et al.) 10 June 1997 (10.06.97) claim 1,4; fig.1-3.	1-5
A	US 5644515 A (SAMPLE et al.) 1 July 1997 (01.07.97) abstract; fig.1A.	1-3
A	US 5963735 A (SAMPLE et al.) 5 October 1999 (05.10.99) claims 1-4; fig.1A.	1-3

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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Name and mailing adress of the ISA/AT Austrian Patent Office Kohlmarkt 8-10; A-1014 Vienna Facsimile No. 1/53424/535	Authorized officer Mihatsek Telephone No. 1/53424/329

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/KR 00/00229

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US A 5329470	12-07-1994	US A 5477475	19-12-1995
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		EP A3 372833	11-12-1991
		JP A2 2245831	01-10-1990
		US A 5109353	28-04-1992
		US A 5329470	12-07-1994
		US A 5477475	19-12-1995
		US A 5644515	01-07-1997